Effect of CMOS Technology Scaling on Fully-Integrated Power Supply Efficiency

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***Abstract*— Integrating a power supply in the same die as the powered circuits is an appropriate solution for granular, fine and fast power management. To allow same-die co-integration, fully integrated DC-DC converters designed in the latest CMOS technologies have been greatly studied by academics and industrialists in the last decade. However, there is little study concerning the effects of the CMOS scaling on these particular circuits. To show the trends, this paper compares the achievable efficiencies of the 2:1 switched capacitor DC-DC converter topology under the same constraints in 65, 130 and 350nm bulk CMOS nodes and 28nm in bulk and FDSOI technologies with various capacitor options.**

Keywords*— *Fully-integrated power supply, switched capacitor converter, on-chip voltage regulator, power management scaling.

I. INTRODUCTION

Power management in embedded systems faces several technical challenges. First, the size of the power supplies which distribute the power from the battery to all circuits cover up to one third of the motherboard surface mainly due to their numerous passive components. Secondly, the recent processing circuits such as multi-core processors need various and fast-modulated power rails to optimize their power consumption [1]. Thirdly, the designer has to deal with the dense power rail routing and numerous dedicated power pins in the high power density circuit packages. Lastly, the power supply validation at system-level is done during the final design stage. To overcome these challenges, *burying the power supply* close to or in the powered circuits is a key solution, and to do this, the power electronics and VLSI communities have to work together to find relevant solutions for dense and efficient in-package or on-chip power supplies.

The power supply in package i.e. point of load (PoL) concept is now widely-used in some embedded systems. In addition, some companies provide small and highly-efficient step-down regulators with integrated power MOSFETs, inductors and capacitors in a single package. To propose a better integration, some work has studied the performance of on-chip power supplies in the last decade. There are two major approaches: i) 3D IC packaging [2,3] and ii) on-die voltage regulators. The first uses dedicated layers to provide high-density passive components stacked with the powered circuits through high density 3D connections. The second approach i.e. the on-die solution, relies on powered circuit technology being suitable for efficient power supply design. Due to the CMOS process limitation [4], inductorless DC-DC converter topology i.e. switched capacitor converter (SCC) has been well studied in the literature [5-7]. Fig. 1 shows the classical Figure of Merit (FoM) (power density v. efficiency) of an on-die SCC published in the last decade [8-24]. However, there is no clear link between the achievable power density and the technology node. Moreover, the technology impact is difficult to distinguish from the design refinements and environment constraints (ratio, input voltage, and power level, etc.). It is therefore clear that comparison of the SCC under the same conditions over a large CMOS technology nodes range has been insufficiently studied [25].

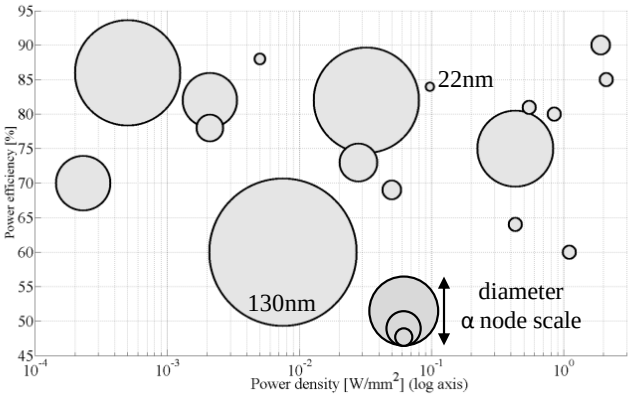

Fig. 1. Power density v. efficiency for different technology nodes

This paper provides a contribution to on-chip power supplies by studying the effect of major CMOS technology nodes on the power supply performance especially the power efficiency of SCCs. First, the SCC losses are described and a model is given to have a physical insight into the efficiency optimization. Based on this analysis, extraction of the key technology parameters is explained. Then, these parameters are given for major CMOS technology nodes. Based on transistor-level simulations and an optimization procedure, the maximal SCC efficiencies are given over a large silicon surface range for three different CMOS technologies (130, 65, 28nm) and capacitor options (MOS, MIM, deeptrench) for a 2:1 converter using a 1.8V input voltage.

II. SCC EFFICIENCY ANALYSIS

A. 2:1 Switched Capacitor Converter Topology

The SCC topology is studied here because of its inductorless property and integration capacity proved in the CMOS process [26]. N to M conversion ratios in SCC topology are possible [27], but 2:1 SCC achieves the best power efficiency. Therefore in this paper, the most efficient SCC

topology is chosen in order to study the maximal achievable efficiency [28], [29]. Other ratios will have lower performance.

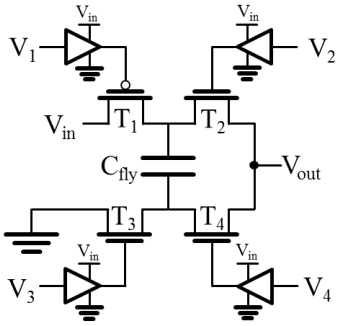

Fig. 2. 2:1 switched capacitor converter (SCC) schematic

The 2:1 SCC reduces the input voltage rail V_{in} to the output voltage V_{out} by a factor of two under ideal and open-circuit conditions. This topology mainly consists of a flying capacitor C_{fly} charged and discharged in two phases by four switches as shown in Fig. 2. In the first phase, ϕ_1, T_1 and T_4 are in on-state and the capacitor is charged from the input voltage through the output load. In the second phase, ϕ_2, the flying capacitor is discharged into the load through transistors T_2 and T_3. Between the two phases, a dead time is introduced to avoid cross-conductions between the output, input and ground terminals.

B. *Efficiency Modelling*

The SCC has inherent losses (*charge-sharing* loss) due to the charge and discharge of the flying capacitor C_{fly} through the on-state resistance of the switches $T_{1,2,3,4}$. [30] has already derived the electrical equations for 1:1 SCC. From this work, the conduction loss P_{cond} for a 2:1 SCC can be expressed as:

$$P_{cond} = \beta \coth\left(\frac{\beta}{2}\right) R_{on} i_{out}^2 \quad (1)$$

where the coefficient β is equal to $\frac{1}{2R_{on}C_{fly}F}$, R_{on} is the on-state switch resistance and F_{sw} is the switching frequency.

The switching nature of the SCC also implies the switching loss P_{sw}. As each switch is commuted once during the switching period, the transistor gates are charged and discharged at F_{sw}. Moreover, the on-die capacitance often has a parasitic capacitance connected between the bottom plate and the ground which leads to additional switching loss. Assuming the four switches have the same size, P_{sw} can then be given by:

$$P_{sw} = 4Q_g V_{in} F + C_{bot} V_{out}^2 F \quad (2)$$

where Q_g is the charge needed to move from off- to on-states.

By definition, the power efficiency is expressed as:

$$\eta = \frac{P_o}{P_o + P_{loss}} \quad (3)$$

where the output power P_o is equal to $V_{out} \times I_{out}$, and P_{loss} is the sum of P_{cond} and P_{sw} losses.

To model a digital load (~1W@1V), an approximate exponential current profile I_{out} is chosen for the following simulations:

$$I_{out} = V_{out}^2 + 0.2V_{out} - 0.1 \quad (4)$$

The designer has to maximize the power efficiency using design freedom parameters: i) the flying capacitor value C_{fly}, ii) the total transistor width W and iii) the switching frequency F_{sw}. In this paper, the design is done from a given silicon area called S. As the switch area is negligible compared to the capacitor size, the C_{fly} value is directly given by:

$$C_{fly} = \sigma S \quad (5)$$

where σ is the capacitance density in F/m^2.

The total loss P_{loss} can be calculated from equations (1), (2) and (5), and by introducing some key technology parameters [26] so that:

$$P_{loss} = \frac{\coth\left(\frac{W}{4\lambda_r \sigma SF}\right)}{2\sigma SF} i_{out}^2 + \left(\lambda_q W V_{in} + \alpha \sigma S V_o^2\right) F \quad (6)$$

where λ_q is the gate charge density (expressed in C/m), λ_r is the on-state resistance density (Ω×m metric) and α is the parasitic to flying capacitance ratio.

Fig. 3 shows the efficiency versus the two design variables {W,F} for a typical CMOS case: λ_q=1fC/µm, λ_r=1kΩ×µm, R_o=1Ω, σ=10nF/mm^2, α=1%, and S=1mm^2. This graph clearly shows an optimal point {W_{opt},F_{opt}} where the power efficiency is maximized. Here, the optimal width and switching frequency are 31600µm and 500MHz, respectively.

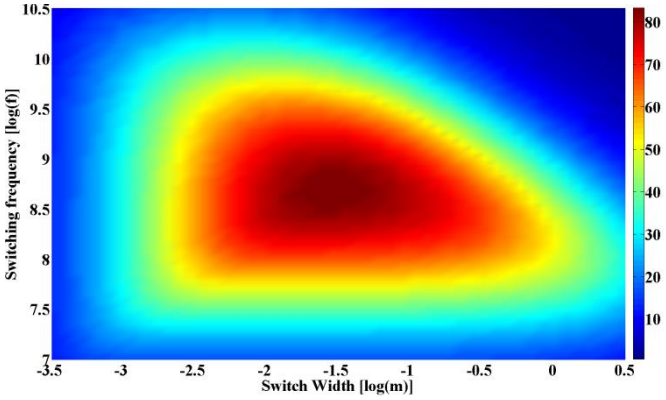

Fig. 3. SCC efficiency v. the two main design variables {W,F}

III. Key Technology Parameters for SCC

As shown in equation (6), the losses are directly related to four critical technological parameters. In this section, the test bench to extract each parameter from a targeted CMOS technology is described in detail.

A. *Parameter Extraction for Switch Properties*

The losses due to the switches are mainly evaluated by the on-state resistance density (λ_r) and the gate charge density (λ_q) in the modeling presented in equation (2). These two parameters are extracted using the schematic given in Fig.4. The on-state current through drain-source transistor is set by the resistance R following the relation $I_{ds} = (V_{in}-V_{ds})/R$ under ohmic regime condition. The drain-source voltage is less than 100mV and Vgs is maximized to maintain the transistor in the

ohmic region. The R_{driver} value is set to maintain the rise time of the gate voltage V_g inferior to the switching period T_{sw}.

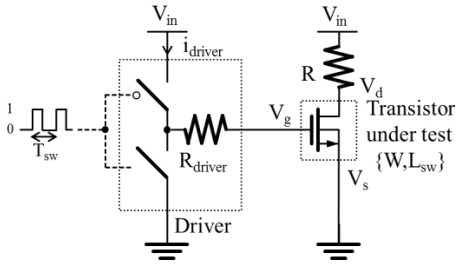

Fig. 4. Schematic for the extraction of the on-state resitance density and the gate charge density

In order to reduce the on-state resistor, the length of the transistor L_{sw} is minimized while the voltage rating is ensured. Using DC analysis, the parameter λ_r is evaluated thanks to the V_d potential when the switch is in on-state so that:

$$\lambda_r = R_{ON} \times W = \frac{V_d}{V_{in} - V_d} \times R \times W \qquad (7)$$

By using a transient analysis, the parameter λ_q is extracted as a result of the energy delivered by the driver to the gate of the transistor during one switching period. Thus, the charge density λ_q is given by:

$$\lambda_q = \frac{E_{Driver}}{V_{IN} W} = \frac{1}{W} \int_{t=0}^{T_{sw}} i_{driver}(t) dt \qquad (8)$$

B. Parameter Extraction for Flying Capacitor Properties

To simplify the capacitor extraction from the complex model given by a technological design kit, we assume the flying capacitor terminals $\{V_{c+}, V_{c-}\}$ are only connected to the bulk by pure capacitors C_{top} and C_{bot} as shown in Fig. 5.a. The extraction of α and σ is done by performing an AC analysis and adding resistance R_m connected as shown in Fig. 5.b. Due to the poly-type capacitor structure [6], only C_{bot} is evaluated because C_{top} is negligible most of the time.

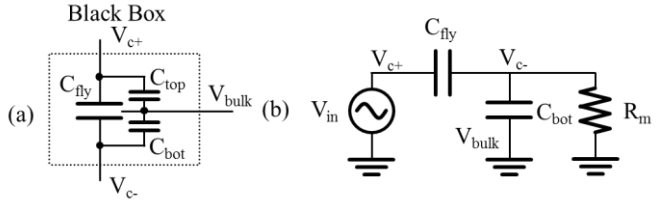

Fig. 5. (a) Equivalent schematic of a flying capacitor and (b) Schematic for the extraction of the capacity density and the parasitic capacity

For MIM and TSC, the C_{top} and C_{bot} parasitic capacitors are negligible compared to C_{fly} by their nature. The equivalent impedance seen by the AC source can be expressed as:

$$Z_{eq}(s) = \frac{1 + R_m(C_{fly} + C_{bot})s}{(1 + R_m C_{bot} s) C_{fly} s} \qquad (9)$$

This equation leads to two cutoff frequencies in the AC analysis which directly determine the C_{fly} and C_{bot} capacitor values by the following expressions:

$$C_{bot} = \frac{1}{2\pi R_m F_{c1}} \text{ and } C_{fly} = \frac{1}{2\pi R_m F_{c2}} - C_{bot} \qquad (10)$$

Then, from (10), α and σ values are given by the following equations:

$$\propto = \frac{C_{bot}}{C} \text{ and } \sigma = \frac{C}{S} \qquad (11)$$

C. Key Parameters for Major Technology Nodes

Using the above extraction procedure, Table 1 gives the most important technological parameters to assess the capacity of achieving the highest efficiency in three widely-used CMOS technologies. The best parameters are highlighted in bold. To be able to work with 1.8V, the transistors have thick oxides. This means that the minimal length for the switch is greater than the minimal length allowed by the process. We therefore assume that TSC geometry density is independent of the technology node [31]. The equivalent serial resistor (ESR) is also not taken into account.

The classical factor of merit, $FoM_s = R_{on}Q_g$, equal to the product of λ_r and λ_q, gives a trend of how close the transistor will be to an ideal switch. Here, the 28nm and 65nm nodes have similar values leading to less transistor contribution on the overall loss expressed in (6), than the 130nm node. The 65nm node has the best poly-type capacitor density with lowest parasitic capacitor ratio. These two facts show that scaling does not necessarily provide better technological parameters to achieve the highest power efficiency. On the other hand, the MIM-option which is not directly linked to a scaling effect provides better capacitor density but needs additional layers leading to extra silicon cost.

TABLE I
PROCESS PARAMETERS INFLUENCING CONVERTER PERFORMANCE

Parameter	130nm bulk	65nm bulk	28nm FDSOI	Unit
MOSFET length L_{sw}	350	250	180	nm
N-MOSFET channel resistivity density λ_r	2.2	0.68	**0.55**	kΩ × µm
N-MOSFET gate charge density λ_q	3	**2.9**	3.2	fC/µm
Figure of Merit of the switch FoM_s	6.7	1.9	**1.8**	kΩ × fC
Integrated poly cap. density $\sigma_{c,poly}$	3.7	**9.6**	6.6	fF/µm²
Bottom plate poly cap. coefficient ∝	4.8	**1.2**	8.6	%
Integrated MIM cap. density $\sigma_{c,mim}$	5	5	**15.9**	fF/µm²
Integrated TSC cap. Density $\sigma_{c,tsc}$	**100**	**100**	**100**	fF/µm²

Note: in bold, the best benefit value in terms of converter design (1) Thick oxide 150nm- and 280nm-long channel transistors in 65 and 28nm technology, respectively; driving voltage 1.8V; (2) Thick oxide polysilicon capacitors at 1.0V bias with 1.8V maximal voltage rating; (3) additional layers needed for MIM (Metal Insulator Metal) capacitor option, the bottom plate of the MIM is negligible. In 28nm, the MIM voltage rating is 1.1V (4) included in the DKit model (not post-layout extracted).

IV. Achievable SCC Power Density

A. Optimization Procedure

The aim of the optimization is to find the highest efficiency for a silicon surface in a 0.1 to 50mm² range. For each given surface S, the capacitor density and chosen capacitor type determine the C_{fly} value. Then, the design freedom couple $\{W_{opt},F_{opt}\}$ is determined by using expressions (3) and (6) in an exhaustive search procedure. After that, we perform a transistor-level simulation to find a more precise couple value. Lastly, the P_o/S ratio is calculated to give the power density at each given surface.

B. Efficiency v. Power Density

Fig. 6 shows the evolution of the efficiency against power density for each capacitor type available in 28nm FDSOI technology. This figure shows the strong influence of the capacitor density and the parasitic capacitance on power efficiency. As the TSC has the better density, as shown in Table 1, the best efficiency is achieved by this capacitor type. The poly-type capacitor has the lowest efficiency due to its low density and high parasitic capacitance ratio α. Another example from Fig. 6 is that using the power density of a converter with TSC is five times better than using the MIM option to reach 80% efficiency.

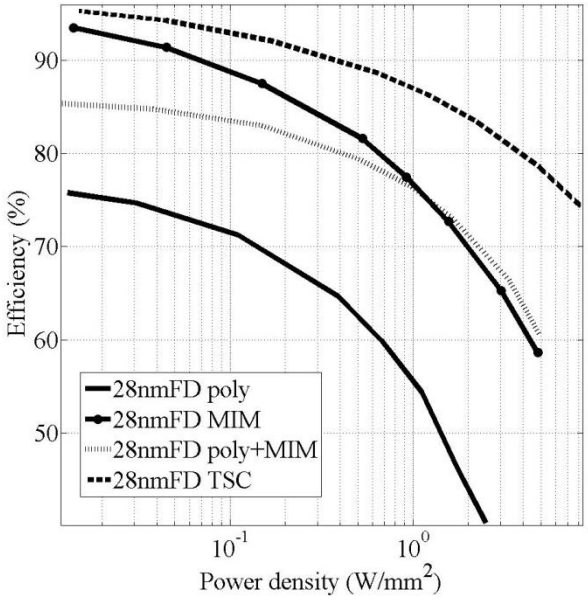

Fig. 6. Influence of the capacitors for the 28nm technology

Fig. 7 shows the efficiency v. power density in the 28nm, 65nm and 130nm technologies for the same capacitor type i.e. TSC in order to only show the $R_{on}Q_g$ impact. Due to the similar $R_{on}Q_g$ FoM_s, see Table 1, the 28 and 65nm nodes achieve similar efficiency. These results show that the thinner node does not necessarily improve the converter performance for the same capacitor density. On the other hand, the 130nm process has the lowest power density because its FoM_s is three times greater than the other technologies. Beyond the length, $R_{on}Q_g$ characterization is needed to determine the technology ability to propose efficient switching properties. Notice the most recent technologies limit the voltage rating capability of the transistor, thus limiting the input voltage value.

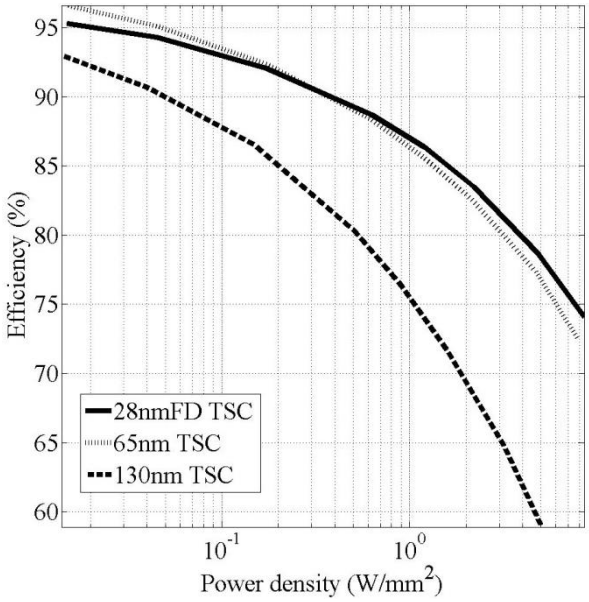

Fig. 7. Influence of the node technology for the TSC capacitors

The evolution of the efficiency against power density for each technology using the available capacitor i.e. a stack of MIM- and poly-types is shown in Fig. 8. Due to the highest MIM capacitor density, the 28nm technology has the best efficiency for any power density. Despite a better $R_{on}Q_g$, the 65nm node gives a similar efficiency to the 130nm one which leads to the conclusion than the capacitance density is the predominant technology parameter.

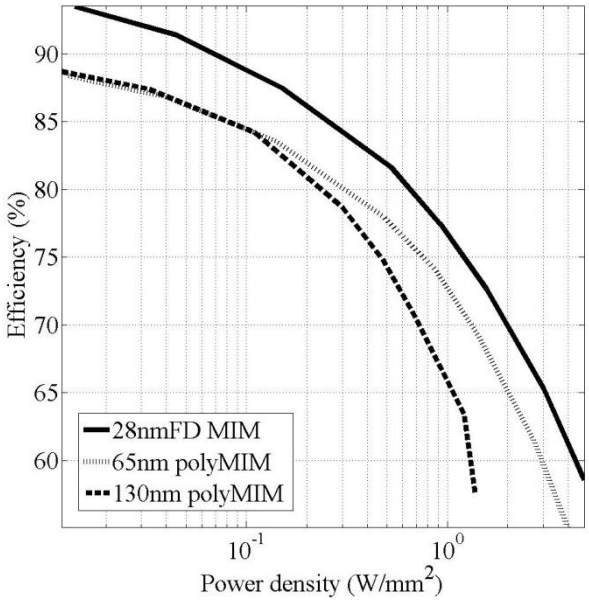

Fig. 8. Influence of the node technology for the MIM- and poly-type capacitors

V. Conclusion

In this paper, we have studied the impact of CMOS scaling on the fully-integrated capacitor-based converter. We have

proposed a compact modeling to highlight the most critical technology parameters which influence the power efficiency. In addition, we have described the procedure to extract these parameters. By using the optimization process based on the proposed models and transistor-level simulation, we have studied three CMOS technological nodes 130, 65 and 28nm. As shown in the simulation results, the capacitor density is the most critical parameter for achieving high power density conversion. Due to the high MIM density in the studied 28nm node, which is not directly linked to the scaling effect, this technology offers the best power density for 1.8V input voltage.

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